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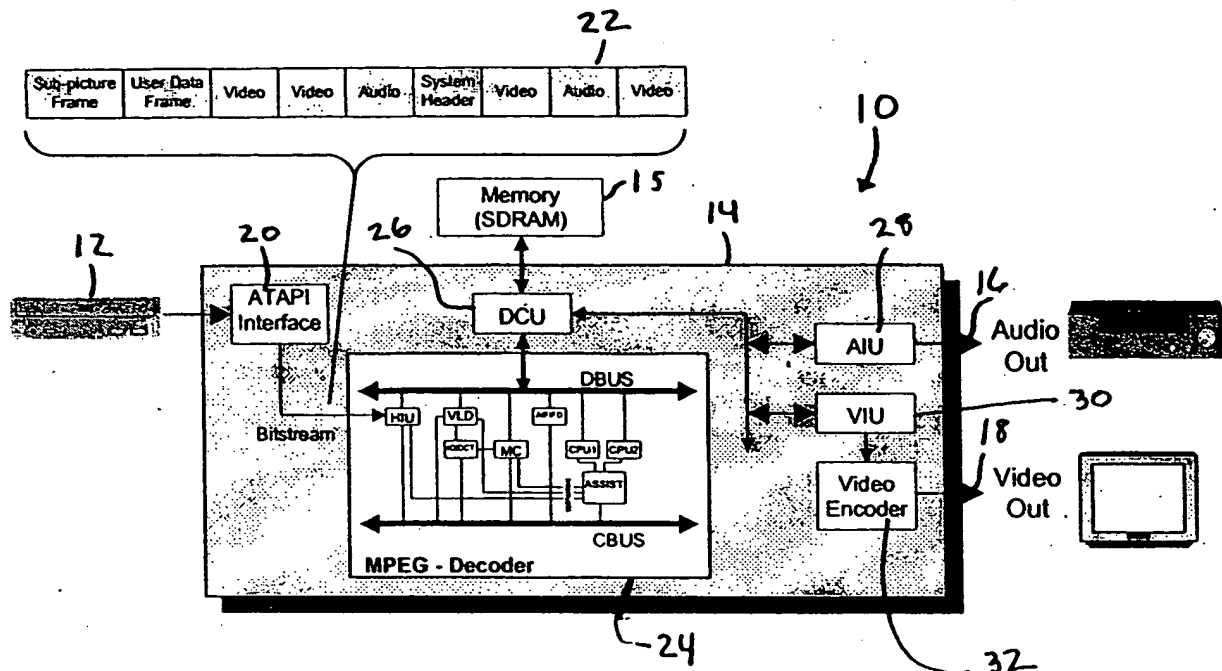


FIGURE 1

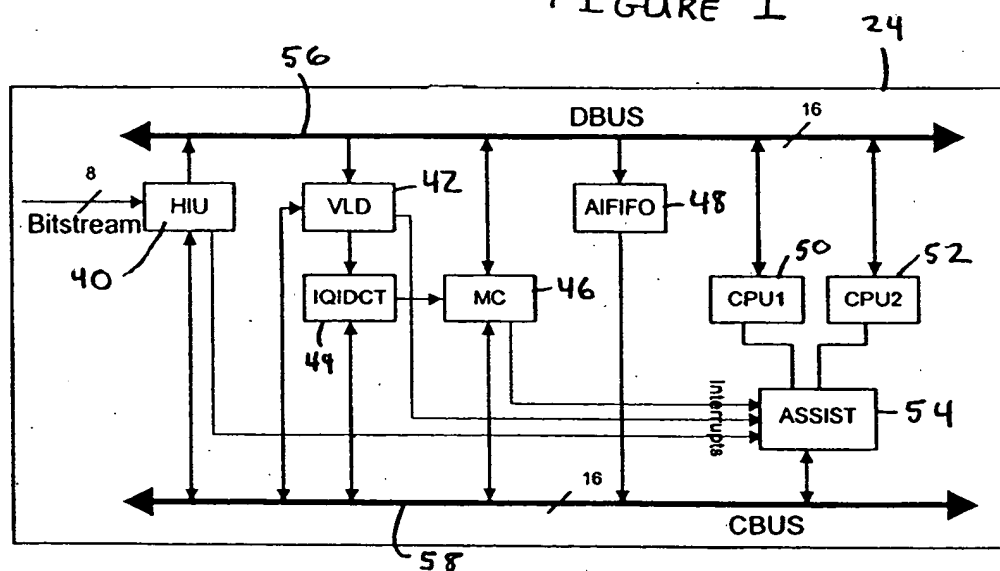


FIGURE 2

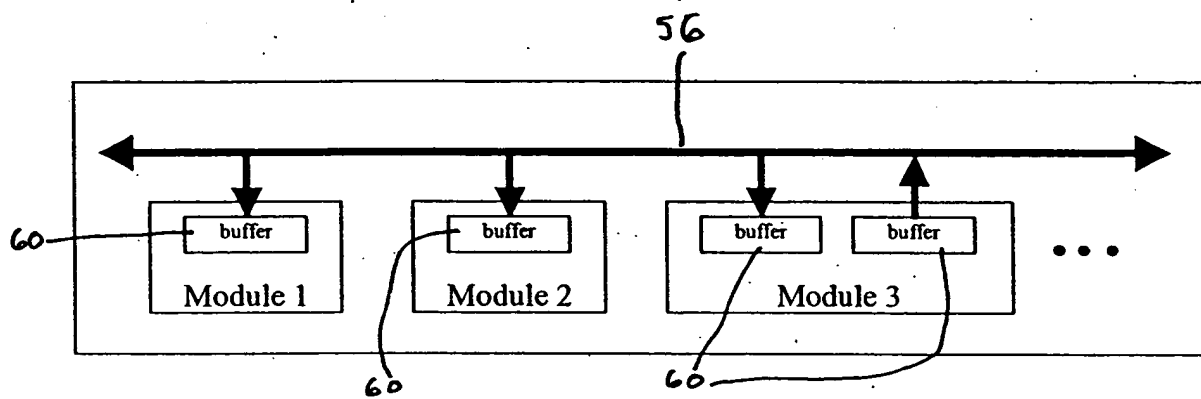


FIGURE 3

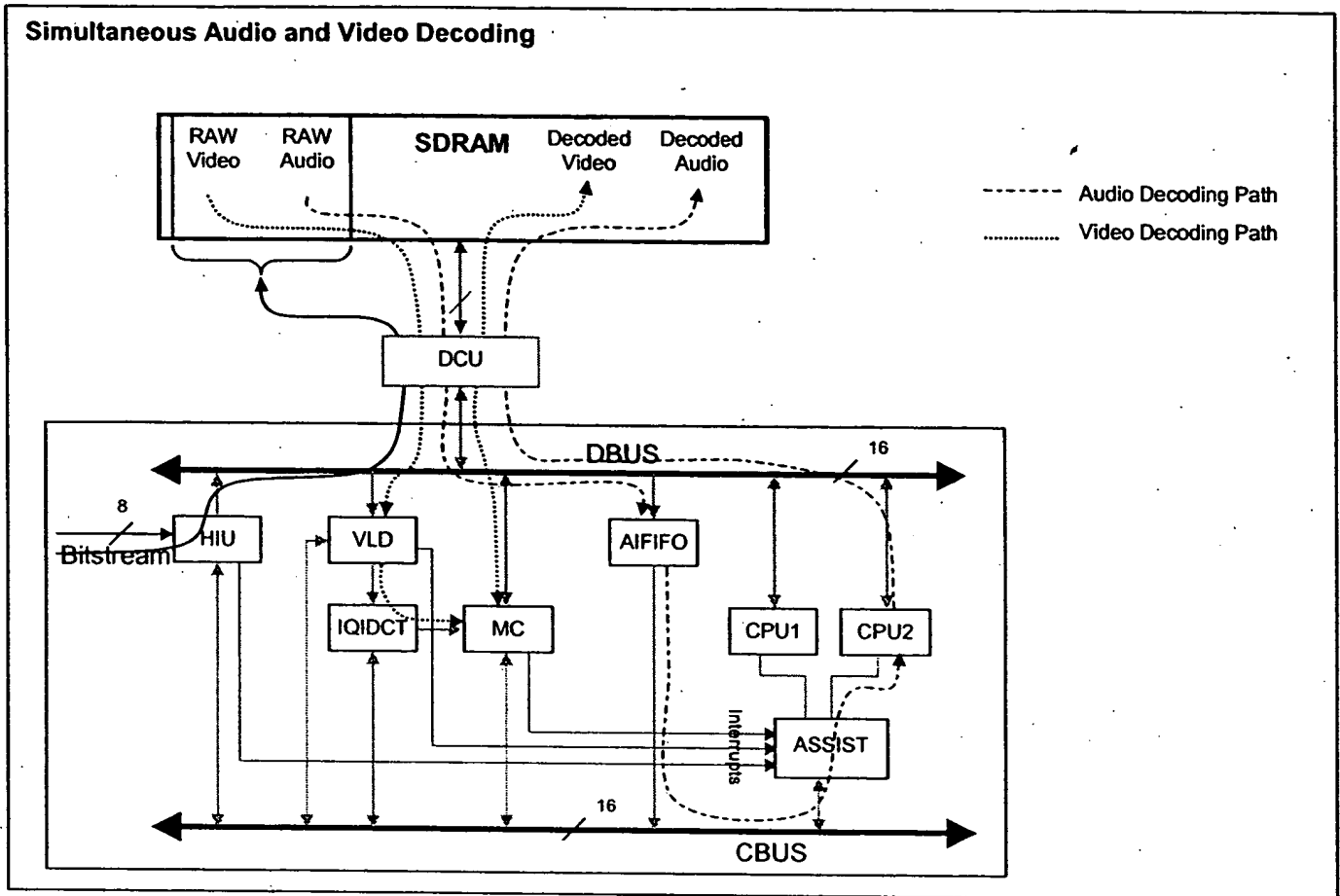


FIGURE 4

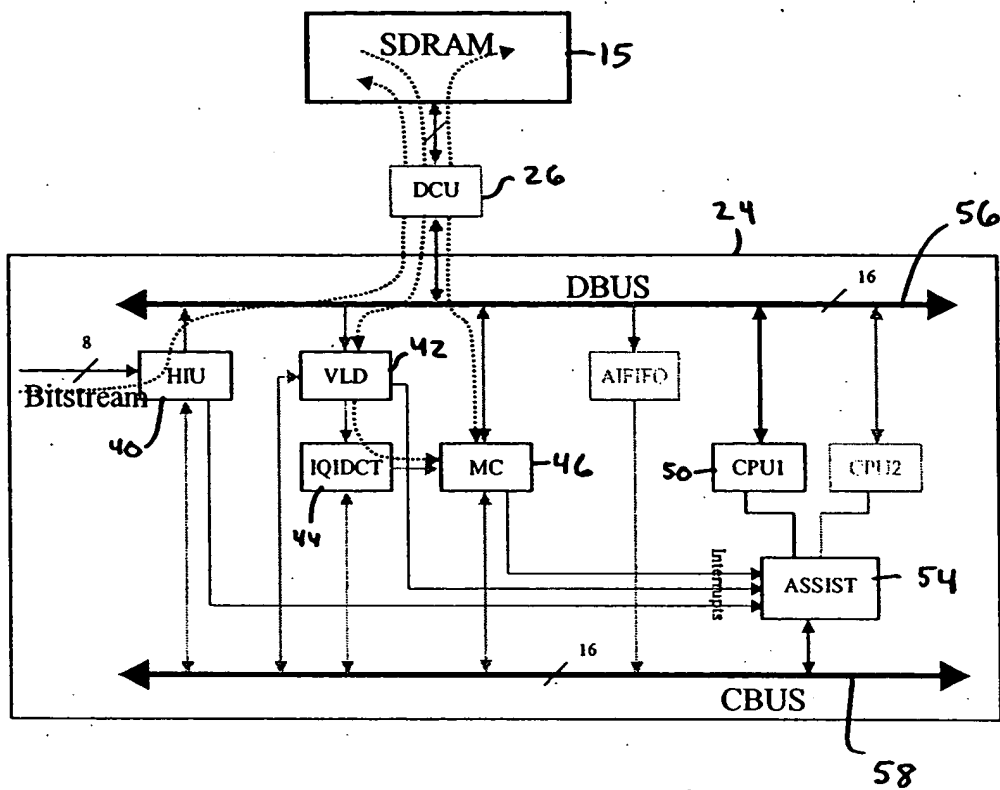


FIGURE 5

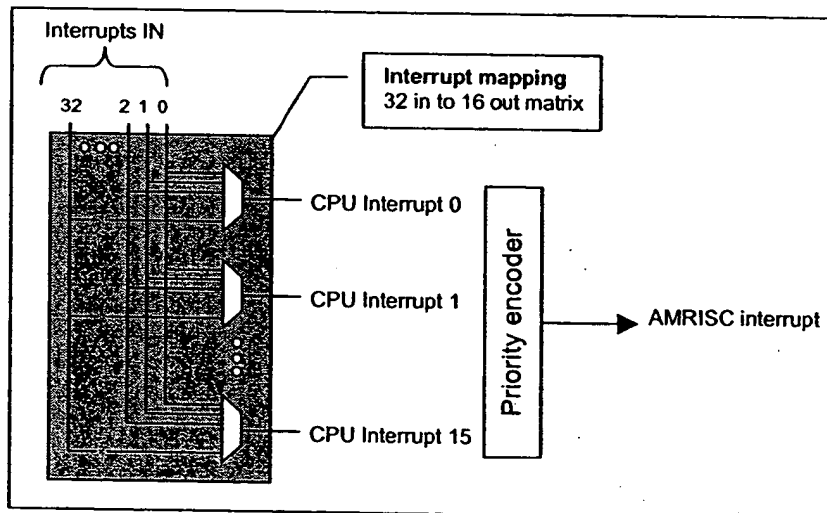


FIGURE 6

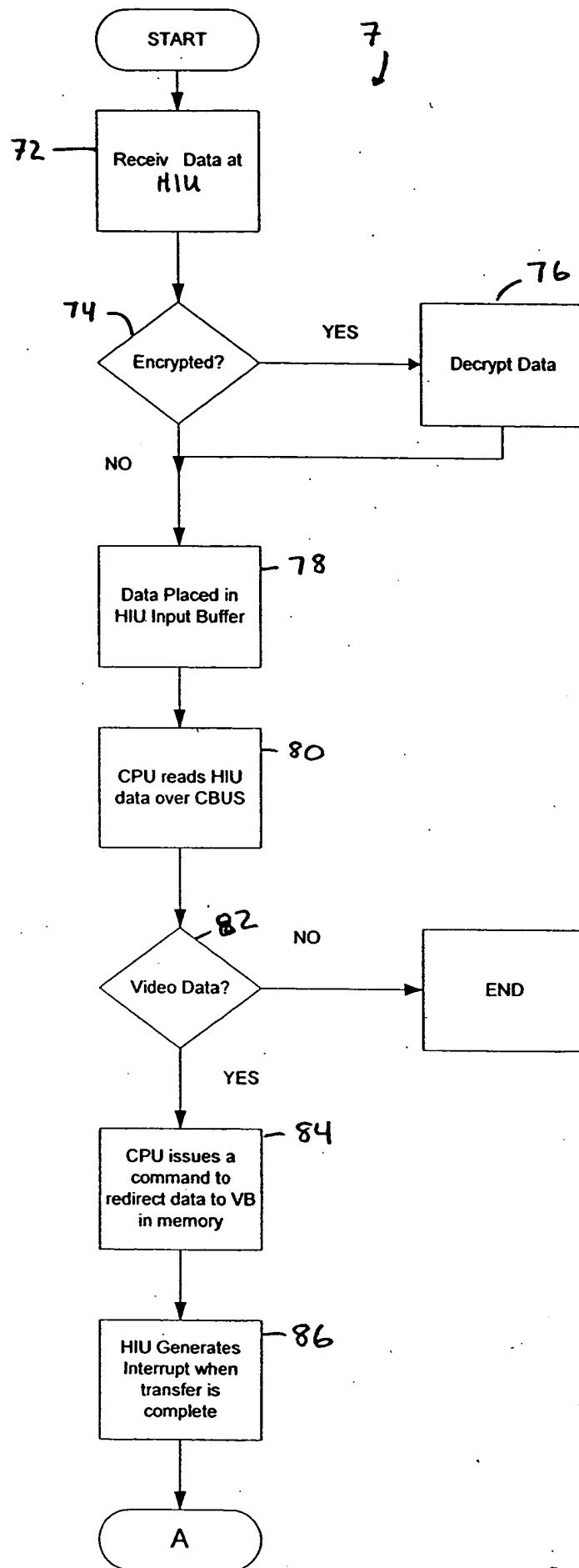


FIGURE 7A

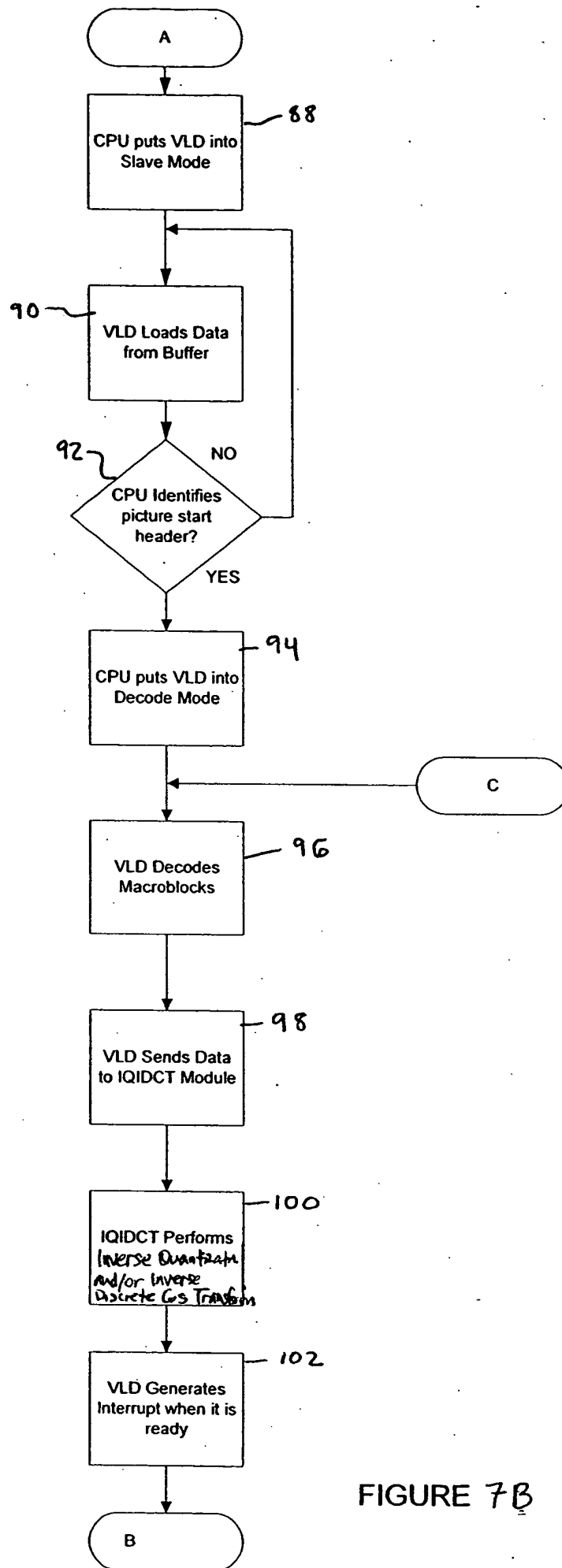


FIGURE 7B

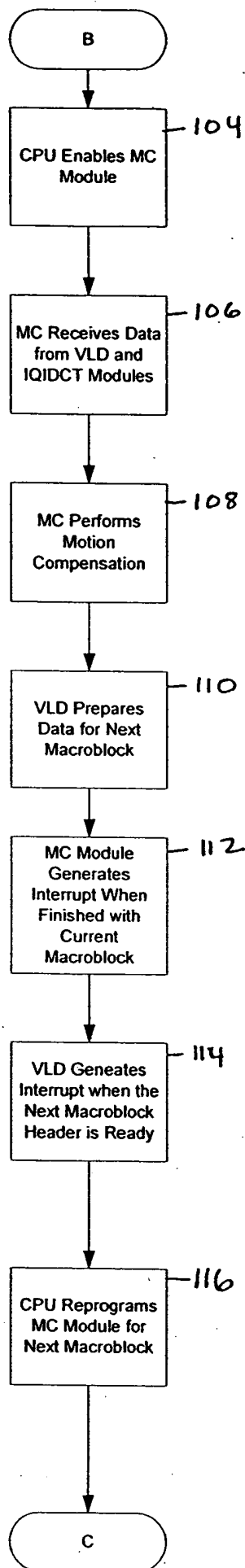


FIGURE 7C

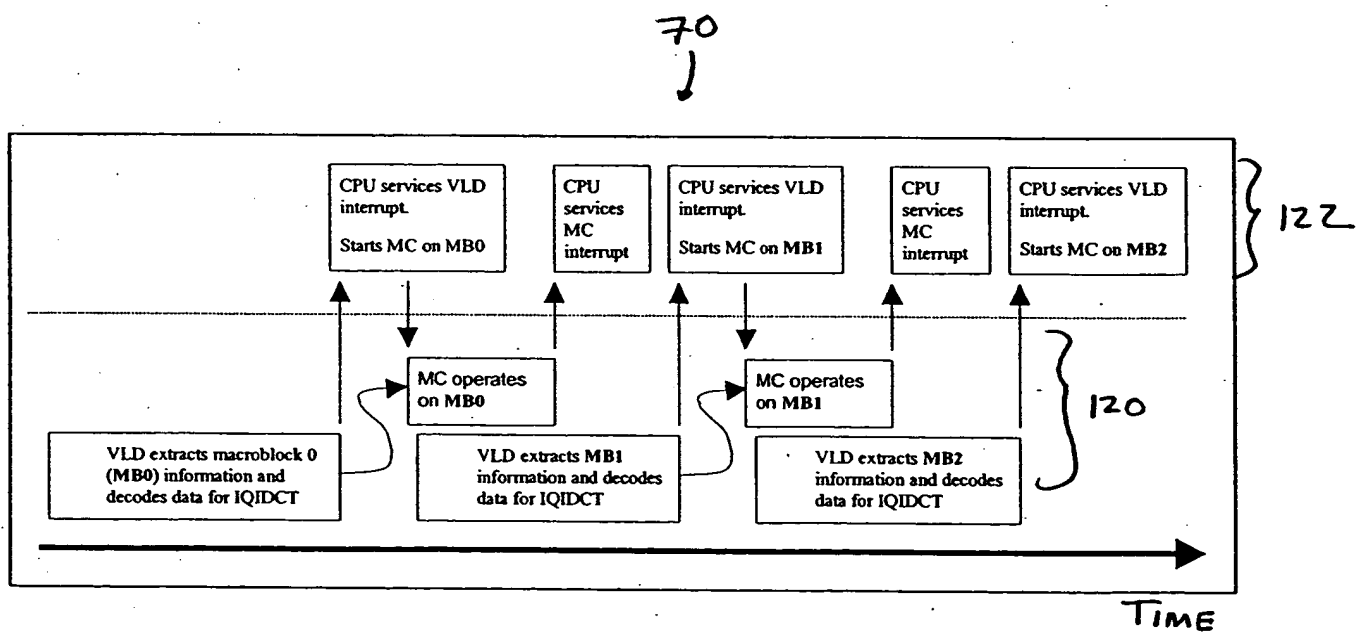
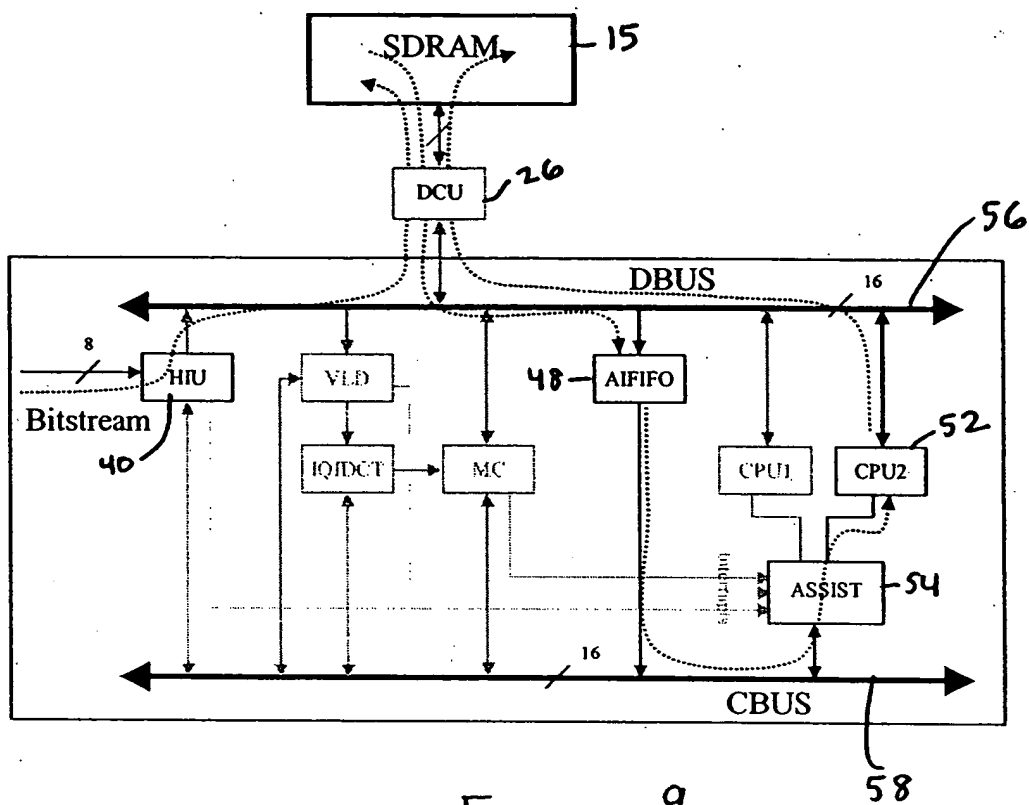


FIGURE 8



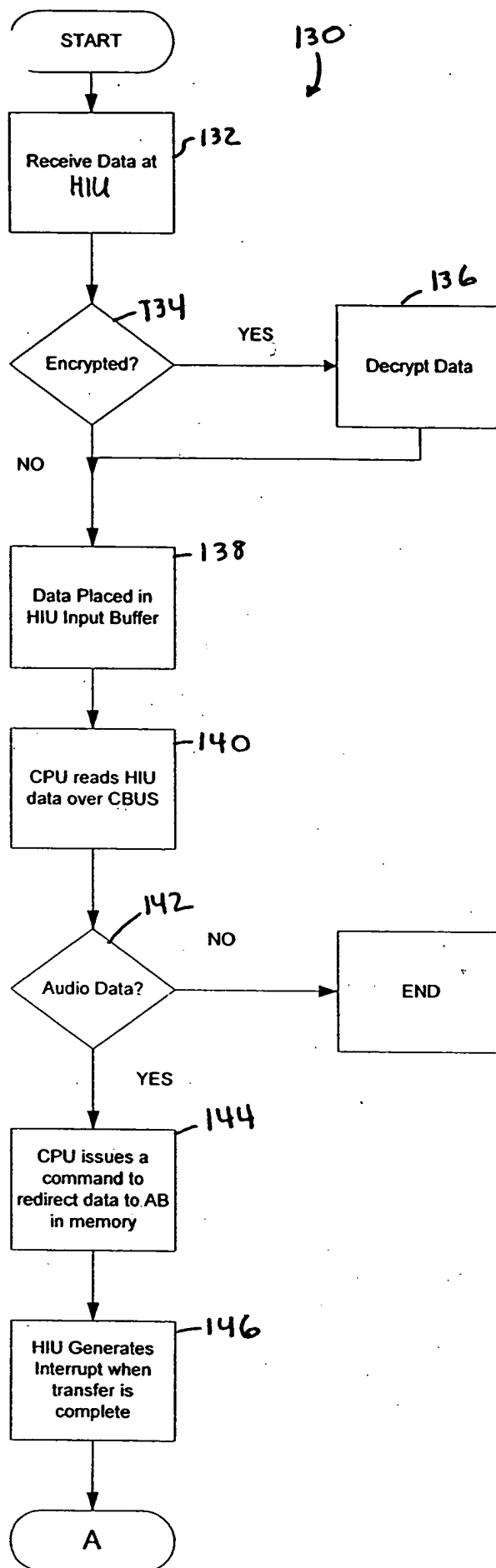


FIGURE 10A

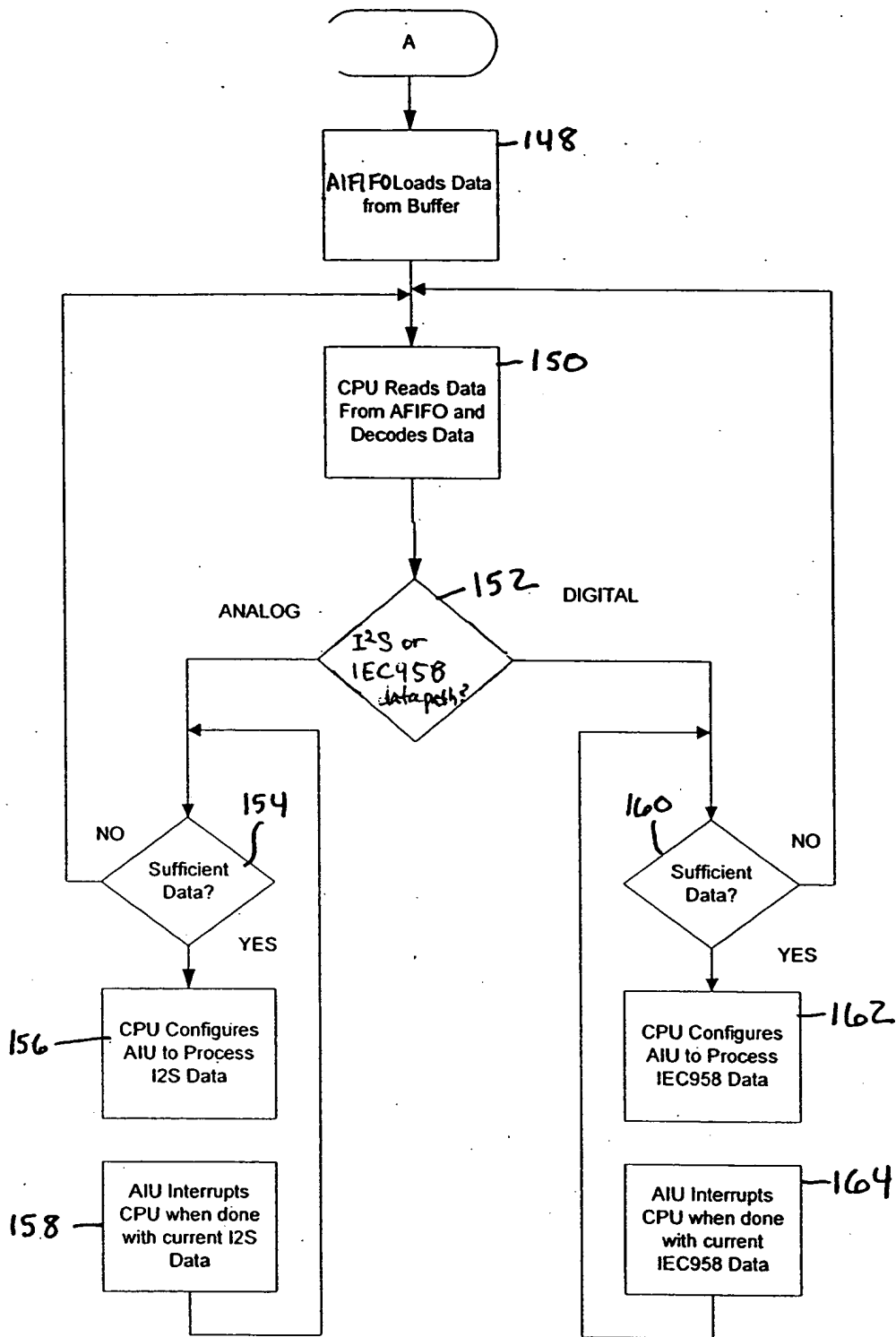


FIGURE 10B

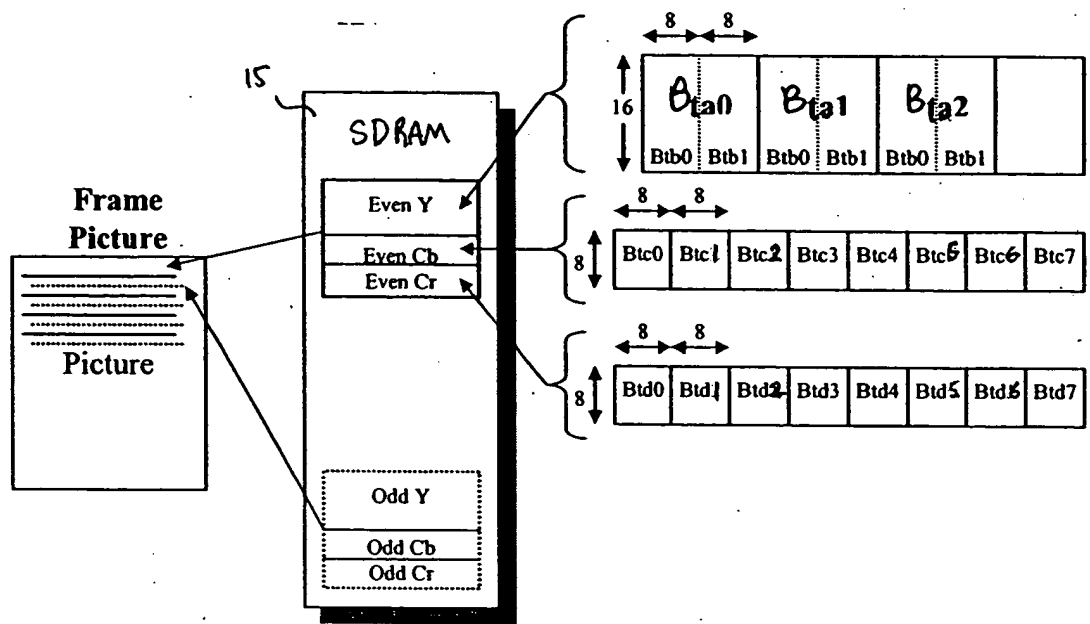


Figure 11: SDRAM Mapping

FIGURE 11

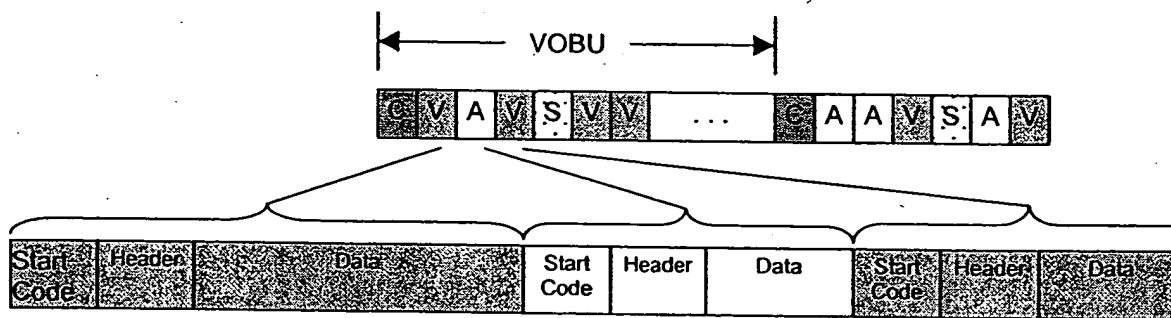


FIGURE 12

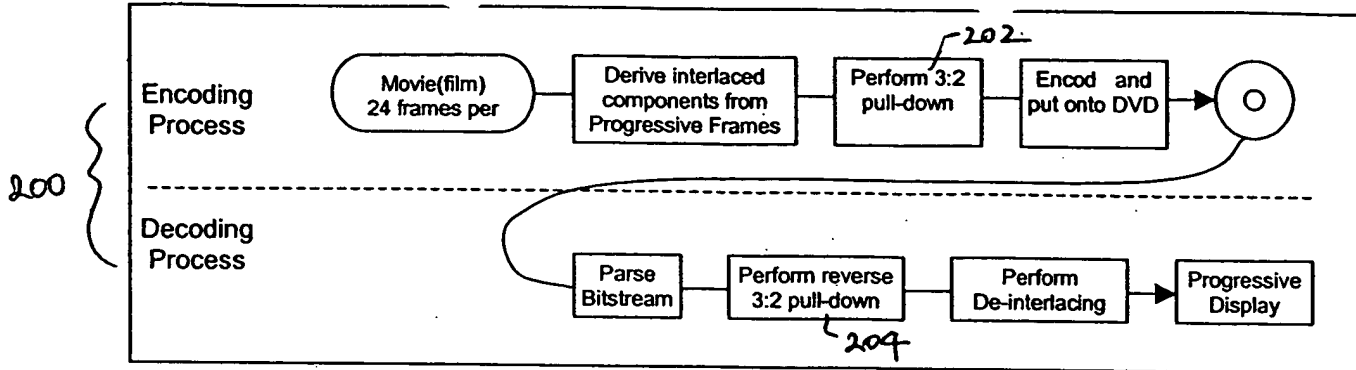


FIGURE 13A

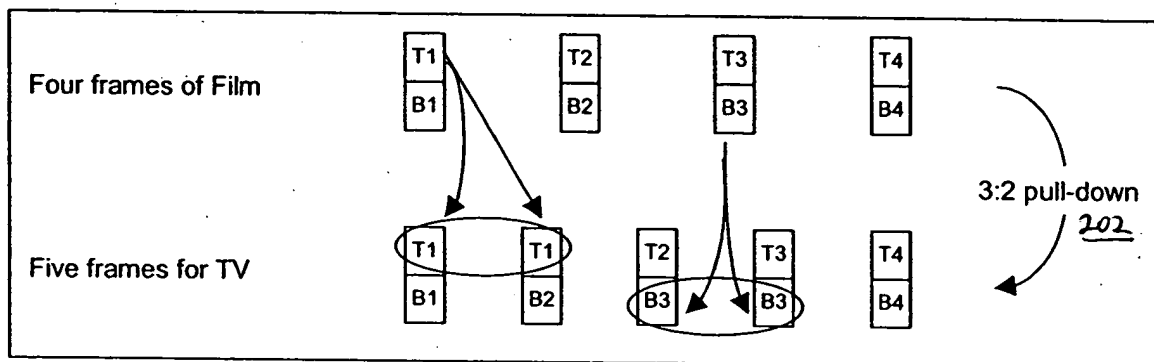


FIGURE 13B

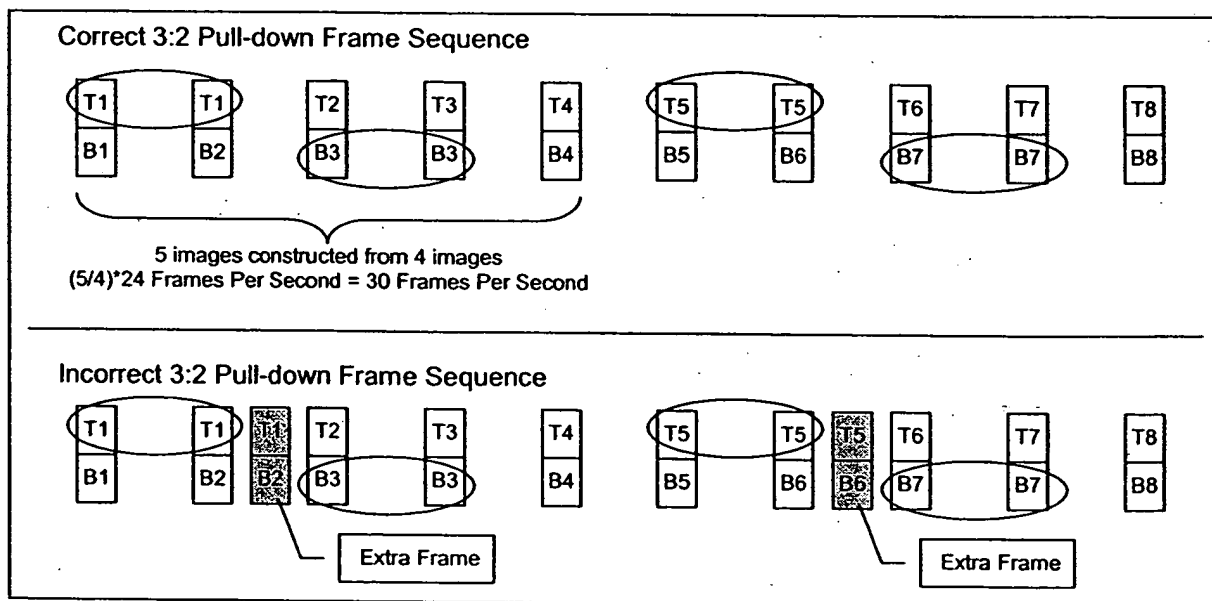


FIGURE 13C